NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. M4065.0082/P082-A
Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS

and invented by:

Paul A. Farrar

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☒ Divisional

☐ Continuation-in-part (CIP) of prior application No.: 09/134,363

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 23 pages(s) and including the following:
   a. ☒ Descriptive title of the invention
   b. ☐ Cross references to related applications *(if applicable)*
   c. ☐ Statement regarding Federally-sponsored research/development *(if applicable)*
   d. ☐ Reference to microfiche appendix *(if applicable)*
   e. ☒ Background of the invention
   f. ☒ Brief summary of the invention
   g. ☒ Brief description of the drawings *(if drawings filed)*
   h. ☒ Detailed description
   i. ☒ Claims as classified below
   j. ☒ Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [X] Formal [ ] Informal Number of sheets: 8

4. [X] Oath or Declaration

   a. [ ] Newly executed (original or copy) [ ] Unexecuted

   b. [X] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [X] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [ ] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [X] Information Disclosure Statement/PTO-1449 [X] Copies of IDS citations

12. [X] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. [ ] Additional enclosures *(please identify below)*:

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

[X] Large Entity [ ] Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	18	- 20 =		x $18.00	
Independent Claims	3	- 3 =		x $78.00	
Multiple Dependent Claims (check if applicable)				[ ]	
Other Fees (specify purpose):					
				BASIC FEE	$690.00
				TOTAL FILING FEE	$690.00

[X] A check in the amount of $690.00 to cover the total filing fee is enclosed.

[X] The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

- [ ] Charge the amount of ______ as filing fee.
- [X] Credit any overpayment.
- [X] Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- [ ] Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: August 14, 2000

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PATENT
Docket No.: M4065.0082/P082-A
Micron No.: 98-0111.01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Paul A. Farrar

Serial No.: Not Yet Assigned
(Divisional application of Ser. No. 09/134,363 under rule 53(b))

Group Art Unit: 2812

Filed: Concurrently Herewith

Examiner: Unassigned

For: METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS

Assistant Commissioner for Patents
Washington, D.C. 20231

FIRST PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

In the Specification:

Page 1, after the title, please insert --This application is a divisional of application Ser. No. 09/134,363, filed on August 14, 1998, now US Patent No. ____, which is hereby incorporated by reference.--

Page 2, line 11, cancel "to a a computer", substitute --to a computer--.

Page 6, line 6, please add --FIGURES 5A-5E show cross-sectional views of a structure fabricated in accordance with another method of the present invention.--

In the Claims:

Please cancel claims 1-39 and 52-67.

Please add claims 68-73.

--68. The semiconductor device of claim 40, wherein said first insulator layer is at least 2 microns thicker than said at least one metal contact.

69. The semiconductor device of claim 40, wherein said metal pad comprises a metal stack comprising four different metal levels.

70. The semiconductor device of claim 69, wherein said metal levels comprise Zirconium, Nickel, Copper and Gold.

71. A semiconductor device formed on a semiconductor substrate having at least one metal contact formed thereon, said semiconductor device comprising:

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and being in contact with the at least one metal contact;

a second insulator layer overlying said at least one metal pad; and

at least one solder contact formed in said second insulator layer and being in contact with said at least one metal pad, said solder contact having a diameter between 2 and 100 microns.

72. The semiconductor device of claim 71, wherein said at least one solder contact has a diameter of approximately 2 microns.

73. A semiconductor device formed on a semiconductor substrate having at least one metal contact formed thereon, said semiconductor device comprising:

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and being in contact with the at least one metal contact;

a second insulator layer overlying said at least one metal pad; and

at least one solder contact formed in said second insulator layer and being in contact with said at least one metal pad, wherein said solder contact is formed by depositing a photoresist layer over said second insulating layer, forming at least one hole in said second insulating layer and the photoresist layer to expose said at least one metal pad, applying a solder layer over the photoresist layer and in the at least one hole to form at least one solder area in the hole which is in contact with said at least one metal pad, and simultaneously removing the photoresist layer and solder layer using a tape liftoff process while leaving said at least one solder contact in contact with said at least one metal pad.--

REMARKS

The specification has been amended to include a reference to prior application Ser. No. 09/134,363, filed on August 14, 1998, as required by 37 CFR 1.78(a)(2). The specification has also been amended to correct a minor typographical error an to add a description of Figs. 5A-5E. No new matter has been entered by these amendments.

Claims 1-39 and 52-67 have been canceled. New claims 68-73 have been added. The pending application now contains claims 40-51 and 68-73. Allowance of the application is solicited.

Dated: August 19, 2000

Respectfully submitted,

By _____

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PATENT
Micron No. 98-0111
Docket No. M4065.082/P082

METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS

Inventor:
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METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN C4 BONDING PROCESS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method of forming micro solder balls for bonding integrated circuits to a module substrate or to a circuit board, using a C4 bonding process. In particular, there is described a method for forming micro solder balls by a tape liftoff process which allows for an increased number and density of input/ouput connections to be fabricated on each integrated circuit chip, module substrate or circuit board.

2. Description of the Related Art

The central processing units (CPUs) of most modern day computers are typically provided on large circuit boards (mother boards) populated with various integrated circuit (IC) chips, such as microprocessor chips and memory chips. These IC chips work in conjunction with one another to perform the functions of the computer. Contacts on the mother board are connected to contacts on the IC chips by the use of multi-chip modules or directly by conventional means, such as solder. The chips are connected to one another by metal patterns formed on the surface of the module or the substrate mother board. These metal patterns provide a conduit for data exchange between the IC chips.

There is a constant need for computers which operate at faster rates. In order to accommodate this need, various techniques have developed to increase the rate (bandwidth) at which data can be processed and transmitted. One of these

involves increasing the circuit complexity of IC circuits which also often results in a larger package for the IC chip and an increase in the number of input/output (I/O) terminals for chip. Since the amount of data that can be accessed from or transferred to an IC chip is directly proportional to the number of I/O lines the chip contains, increasing the number of I/O terminals directly increases data transfer and processing speed.

IC chips have traditionally been packaged in modules before they are bonded to a mother board or other circuit board. The module consists of one or more IC chips bonded to a module substrate. The composite IC chip-module substrate is then bonded to a a computer mother board or other circuit board. Although this is the traditional method of attachment, recently IC chips have also been directly bonded to mother boards.

Traditionally, IC chips were connected to the first level metal pattern on a module substrate with fine wires (wire bonding). This method of connection was limited by the number of pads which could be placed on the periphery of the IC chip. Since then, considerable progress has been made in reducing the IC chip pad size, thereby increasing the number of pads. However, this technology is still limited by the number of pads which can be formed on the chip periphery, and therefore the number of I/Os on a chip is likewise limited. Therefore, other techniques have been developed over the past 30 years to increase the number of available I/O terminals and eliminate alignment problems.

One of these techniques, known as Controlled Collapse Chip Connection (C4), was developed in the 1960s to deal with the problems associated with alignment of integrated circuit chips on a substrate of a module. This process also sought to increase the number of available I/O terminals which could be available for each IC chip. The C4 process uses solder bumps deposited on flat contacts on

the IC chips to form the bond between the IC chip and the module substrate. The contacts and solder balls on the IC chips are matched with similar flat contacts on the module substrate to form the connection. Once the chip is placed on top of the contacts of the module substrate, the entire device is heated to a temperature which melts the solder. Then, the solder is allowed to set, and a reliable bond is formed between the chip and the module substrate. Although the C4 bonding process is usually employed to bond an IC chip to a module substrate, it can also be used to bond an IC chip directly to a mother board or other circuit board.

One of the main advantages of this process is that the IC chip self-aligns itself on the module substrate based on the high surface tension of the solder. In other words, the chip need not be perfectly aligned over the contacts of the substrate, as long as it is in close proximity the melting of the solder will align the chip with the substrate contacts. The other advantage of this process is that an increased number of I/O terminals can be fabricated for each IC chip. This type of bonding process is also often referred to as "flip-chip", or "micro-bump" bonding. The process can be briefly explained with reference to Figures 1 and 2.

Figure 1 shows a side view of a IC chip 10 and a module substrate 20. The IC chip 10 is fabricated with various metal pattern lines and contacts 50 imprinted on its last metal level, as shown in Figure 2. Formed beneath the IC chip 10 is an array of solder balls 30. The module substrate 20 includes metallized paths 60 for carrying signals from the IC chip 10 to other elements mounted on the substrate. These paths have contacts which match the contacts located on the underside of the IC chip 10. When the IC chip 10 is ready to be mounted, it is placed on top of the module substrate 20 above the substrate contacts with the solder balls 30 attached to the contacts of the IC chip resting on the contacts of the module substrate, as shown in Figure 1. When the device is heated, the solder melts and the chip 10 self-aligns with the module substrate contacts. The solder later hardens

to form a reliable bond between the two sets of contacts. Figure 3 shows the device after the solder has been heated and set. The completed module is then bonded to a mother board (not shown) through wire bonds or additional C4 connections at the module terminals.

Traditionally, the contacts and solder balls have been formed on the IC chip using metal mask technology. In this process a metal mask (essentially a metal plate with a pattern of holes therein) is placed over an IC wafer containing many IC chips 20 for forming the contacts and solder balls. Then, contact material and solder are evaporated through the holes onto the wafer. The holes in the metal masks must be of sufficient size to prevent warpage and damage of the mask during use. Hence, the number of contacts that can be fabricated through use of a metal mask is limited because the holes in the mask must remain above a minimum size to prevent these problems. Consequently, the size of the solder balls that can be created is similarly limited.

The minimum diameter of a C4 solder ball that can be achieved using current techniques, such as metal mask, is approximately 100 microns. Since the size of the solder balls is directly related to the number and density of I/O terminals that can be fabricated on a given IC chip, a decrease in solder ball size would provide for an increase in the number and density of the I/O terminals. This would, in turn, allow for a significant increase in data transmission rates because of the increased number of I/O ports for the packaged IC circuit.

Hence, there is currently a need for a process for forming C4 solder balls which are less then 100 microns in diameter.

SUMMARY OF THE INVENTION

The present invention provides an improved method for forming solder balls used in a C4 bonding process. The present inventor has discovered that by using a tape liftoff process to form the solder contacts, significantly smaller contacts can be easily formed on an IC chip.

The invention is a method of fabricating contact terminals and solder balls on an IC chip. The fabrication utilizes a tape liftoff process to remove unwanted solder and photoresist. Use of the tape liftoff process allows formation of solder balls which are at least two orders of magnitude smaller than prior art solder balls.

Although initially envisioned for use as a replacement for the presently used processes for forming C4 type connections on IC chips, the same process of the invention can also be used to form solder ball connections on module substrates or circuit board substrates.

The above and other advantages and features of the present invention will be better understood from the following detailed description of the preferred embodiment of the invention which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 shows a cross-sectional view of a prior art integrated circuit package before C4 bonds are created.

FIGURE 2 shows a top view of a prior art integrated circuit package before C4 bonds are created.

FIGURE 3 shows a cross-sectional view of a prior art integrated circuit package after the C4 bonds are created.

FIGURES 4A-4Q show cross-sectional views of a structure fabricated in accordance with the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present inventor has discovered that by using a tape liftoff process for screening solder balls onto a substrate, the size of the solder balls can be significantly decreased. The process described below can be used to deposit solder balls on an IC chip, a module substrate, a circuit board, or any similar substrate. Tape liftoff processes, per se, are known in the art, as evidenced by U.S. patent 5,240,878 to Fitzsimmons, which is incorporated herein by reference. Tape liftoff processes are frequently used to remove unwanted photoresist levels once an imaging and etching has taken place.

The process of the invention is explained below with reference to Figures 4A-4Q. Although the following explanation refers to a technique for placing solder balls on a wafer, those skilled in the art will recognize that the process described below can be performed on a single chip. Further, it will also be apparent to those skilled in the art that the process described below can be used to form solder balls on a module substrate or a circuit board (e.g. a computer mother board).

Figures 4A-4Q illustrate the inventive process steps used to create micro solder balls on an IC wafer 110. Figure 4A shows the first stage in the formation of the micro solder balls on the wafer 110. At this stage, an insulating layer 120, such as silicon dioxide (SiO_2), is deposited on the next to last layer of metallurgy

130 of the wafer 110 by a process such as chemical vapor deposition (CVD). Although CVD silicon dioxide is preferred for the first insulating layer, other insulators (e.g., polyimide, silicon nitride, flourinated silicon dioxide) known to those skilled in the art may also be used, and deposited by conventional techniques. The insulating layer 120 should be applied so that its thickness is at least 2 microns greater than the thickness of the next to last metal layer 130. Then, the structure 100 is planarized using a chemical mechanical polishing process (CMP). The resulting device, after polishing, is as shown in Figure 4B, where the excess insulating material has been smoothed away.

Next, as shown in Figure 4C, a first layer of photoresist 125 is deposited over the insulating layer 120. This photoresist layer 125 may be made of any type of photoresist known to those skilled in the art. The photoresist layer 125 is patterned and exposed to create via holes 140, as shown in Figure 4D. The via holes 140 are then used to etch into and remove portions of the insulating layer 120. Figure 4E shows the device after the photoresist layer 125 has been exposed, the via holes 140 have been etched, and the photoresist layer 125 has been removed. These via holes 140 provide a connection for upper conductive levels to the next to last layer of metallurgy 130.

Next, solderable metal pads 150 are formed on the upper surface of the insulating layer 120. This is accomplished by depositing a second photoresist layer 145 on the planarized insulating layer 120, which will be used as a first liftoff layer. Figure 4F shows the device 100 after the photoresist layer 145 has been placed over the insulating layer 120. An insulator such as polyimide may also be used in place of the photoresist layer 145, but it has been found that photoresist provides the best results in the present invention. This photoresist layer 145 should be approximately 1.5 microns thick. After it is deposited, the photoresist layer 145 is patterned and etched down to the insulating layer 120 leaving exposed those areas

on layer 120 where the metal pads 150 are desired, as shown in Figure 4G. Then, a metal stack consisting of Zirconium (Zr), Nickel (Ni), Copper (Cu), and Gold (Au) is formed overtop of the entire device 100 including over the remaining areas of photoresist layer 145 and in the etched areas. This stack is formed by applying the four different metals, one at a time. Such a process is known in the art and described in U.S. patents 5,719,090 and 5,457,345, both to Cook et al., which are incorporated herein by reference. The Gold layer is optional in the metal stack, but provides excellent protection against oxidation. The thicknesses of each layer of metal is preferably approximately: 500 Angstroms of Zr, 750 Angstroms of Ni, 5000 Angstroms of Cu, and 750 Angstroms of Au, although these thicknesses are not critical. These metal layers are deposited to form metal stacks 150 in the etched areas of the photoresist layer 145, and to form excess metal stacks 150' on top of the photoresist layer 145.

Since the photoresist layer 145 and the metal layers 150, 150' are applied over the entire surface of the device 100, it is necessary to remove the unwanted metal 150' and photoresist 145 prior to the next process step. Figure 4H shows the device 100 after all metal layers have been deposited. The excess metal areas 150' which lie overtop of the photoresist layer 145, must now be removed. This is accomplished by a liftoff process. Liftoff processes are a well known method for removing unwanted portions of a device under fabrication. The present inventor has found that a tape-assisted liftoff process is especially beneficial in the disclosed process. The tape utilized is an adhesive-backed polymer, which is applied overtop of the entire metallized resist layer, so that it contacts metal stacks 150'. The tape bonds to the metal stacks 150', which is, in turn, bonded to the photoresist layer 145. The removal of the tape causes all of the metal 150' and photoresist 145 to be stripped away, leaving metal pads 150 in only those areas which were previously etched in the photoresist layer 145. The resulting device 100 after the tape liftoff appears as shown in Figure 4I.

After the metal pads 150 have been formed, a second insulating layer 160 is added overtop of the device 100, as shown in Figure 4J. This insulating layer 160 can be formed of conventional insulating material, such as polyimide, and should be approximately 1.5 microns thick. Although polyimide is preferred for this layer, any insulator known to those skilled in the art may be used (e.g., silicon dioxide, silicon nitride, flourinated silicon dioxide).

Figure 4K shows the next step where a third photoresist layer 170 is deposited for use as a second liftoff layer. This photoresist layer 170 can be a continuous layer of photoresist as shown in Fig. 4K, or can alternatively comprise a 'hard mask' layer. The 'hard mask' design is shown in Figure 4Q, where a 500 Angstrom layer of silicon nitride (Si_3N_4) 175 is sandwiched between two photoresist layers 176 and 177. The upper most photoresist layer will be approximately 0.5 microns thick, with the underlying photoresist layer being thick enough so that the entire stack (i.e. layers 175-177) is thicker than the layer of solder which will be subsequently deposited. In the embodiment described herein, the lower level of photoresist 177 is approximately .5 microns thick. When using the continuous photoresist layer shown in Figure 4K, the photoresist must be at least as thick as the layer of solder which will be subsequently applied (i.e. approximately 3 microns). When using the 'hard mask', however, the photoresist layers 176, 177 need not be that thick, as long as the entire stack is thicker than layer of solder to be applied. Although photoresist has been found by the inventor to provide the best results, the second photoresist layer 170 may alternatively comprise a peel-away insulator, such as photosensitive polyimide.

As shown in Figure 4L, the second photoresist layer 170 is exposed and patterned to produce through holes 180 in the areas above the metal pads 150. Then, the insulator 160 is etched through the holes 180 so that the metal pads 150 are exposed, as shown in Figure 4M.

Next, as shown in Figure 4N, a layer of solder 190 is deposited over the entire device 100. The solder should be deposited so that it is at least 2.33 microns thick. This process produces solder contacts 200 in the through holes 180. The photoresist layer 170 and the solder layer 190 are removed using the tape liftoff process described above with reference to photoresist layer 145. The solder layer 190 and the photoresist layer 170 are lifted away from the insulating layer 160 by an adhesive tape which is applied overtop of the solder layer 190. The tape is an adhesive backed polymer which is applied to the solder layer 190 and subsequently stripped off to remove the unwanted solder 190 and photoresist 170 layers. Since the solder layer 190 will bond to the photoresist layer 170, the stripping action causes both layers (i.e. 170 and 190) to be removed simultaneously.

Figure 4O shows the device 100 after the unwanted photoresist and solder have been removed. Solder contacts 200 which connect with metal pads 150 now project out of the top surface of insulating layer 160. In the final step, the solder contacts 200 are heated to allow them to reflow. When the solder contacts 200 are reflowed they form solder ball contacts 210 having a shape similar to that shown in Figure 4P. These solder ball contacts 210 are composite contacts, including both the flat contact portion and the solder ball portion in a single unit.

In an alternate embodiment of the the present invention, a single liftoff procedure is used to form both the metal pads 150 and the solder ball contacts 200, instead of the multiple liftoff procedure descibed above. This embodiment is useful where only contact pads are to be formed in the last metal layer 130 (i.e. the pad metallurgy). This alternate process will now be explained with reference to Figures 4(E) and 5(A-E).

After step 4(E), instead of depositing a photoresist layer 145 (shown in Fig,4(F)), a thicker photoresist layer 300 is applied overtop of the entire surface of

the device 100 (See Fig. 5(A)). Then, as shown in Figure 5(B), holes 310 are formed in the photoresist 300. These holes 310 are selected according to the desired size of the solder ball contact (i.e. the larger the holes 310, the larger the diameter of the solder ball contact). As shown in Figure 5(C), the metal pads 320 (150 in Figure 4(H)) and the solder ball contacts 330 (200 in Figure 4(O)) are deposited in the holes 310 formed in the photoresist 300 in a single step. First, the metal pads 320 comprising the layers of Zr, Ni, Cu, and Au are deposited by the process described above with reference to Figure 4(H). Then, a layer of solder 330 is deposited. The ensuing liftoff process remove all the excess solder and pad metal to create a device like the one shown in Figure 5(D). The stack 340 which is formed is a composite stack, with the four-layer metal pad on the bottom and solder on the top. The entire stack 340 is then reflowed to form the solder ball contacts 350 shown in Figure 5(E).

Because these solder ball contacts in the invention are formed by deposition of solder through fine closely spaced holes in a photoresist layer and by using a tape liftoff process, rather than a metal mask process, the size of the contacts is decreased significantly. Solder contacts formed using the above process are approximately 2 microns in diameter. This is a significant improvement over prior art solder ball contacts, which are currently 100 microns in diameter. Although the above process can be used to form solder contacts which are approximately 2 microns in diameter, it can also be used by those skilled in the art to produce solder contacts of any size, but particularly those in the range of 2 microns to 100 microns. For example, it might be desirable to form solder contacts of 10, 25, 50 or 75 microns, or any other size in the range of 2 to 100 microns, or in a narrower range such as less than 50 microns, or less than 25 microns, or less than 10 microns, as non-limiting examples.

When producing multiple chips on a wafer, the wafer can be diced, after the solder ball contacts 210 are formed over the entire wafer, to create a multitude of chips with solder ball contacts 210. These individual chips can then be attached to a module substrate or circuit board using the C4 process described above with reference to Figures 1-3.

While the invention has been described and illustrated with respect to forming solder contacts on an integrated circuit chip, it should be apparent that the same processing techniques can be used to form solder contacts on a module substrate, a printed circuit board or other conductor bearing substrate.

Moreover, it should be readily understood that the invention is not limited to the specific embodiments described and illustrated above. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed is:

1. A method for forming solder areas on electrical contacts of a device, said method comprising the steps of:

depositing a photoresist layer on a surface of said device containing said contacts;

forming respective holes in the photoresist layer to said contacts;

applying a solder layer on top of the photoresist layer and in the holes to form solder areas in the holes which contact with said contacts; and,

removing the solder layer on top of the photoresist layer and the photoresist layer using a liftoff process while leaving the solder areas on the contacts.

2. The method of claim 1, wherein the liftoff process is a tape liftoff process.

3. The method of claim 2, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer on top of the photoresist layer, and stripping away said tape to remove the solder layer and the photoresist layer while leaving said solder areas.

4. The method of claim 1, wherein the solder areas are reflowed to form solder ball contacts.

5. The method of claim 1, wherein said device is an integrated circuit wafer and the surface is the surface of said wafer.

6. The method of claim 1, wherein said device is an integrated circuit and the surface is the surface of said integrated circuit.

7. The method of claim 1, wherein said device is a circuit board and the surface is the surface of said circuit board.

8. The method of claim 1, wherein said device is a module substrate and the surface is the surface of said module substrate.

9. A process for forming a solder area on a semiconductor device comprising the steps of:

depositing a first insulating layer on at least one metal contact on a surface of said semiconductor device;

forming at least one first hole in the first insulating layer so that the at least one metal contact is exposed;

depositing metal in said at least one first hole and on top of the insulating layer to from at least one metal pad on the surface of the insulating layer;

depositing a second insulating layer over said device including over said at least one metal pad;

depositing a photoresist layer over said second insulating layer;

forming at least one second hole in the second insulating layer and the photoresist layer to expose said at least one metal pad;

applying a solder layer over the photoresist layer and in the at least one second hole to from at least one solder area in the second hole which is in contact with said at least one metal pad; and,

removing the photoresist layer and solder layer from the device using a liftoff process while leaving the solder area in contact with said at least one metal pad.

10. The process of claim 9, wherein the liftoff process is a tape liftoff process.

11. The process of claim 9, wherein the second insulating layer is polyimide.

12. The process of claim 9, wherein the first insulating layer is silicon dioxide.

13. The process of claim 9, wherein the photoresist layer is at least 2 microns thick.

14. The process of claim 9, wherein the first insulating layer is planarized before the at least one first hole is formed.

15. The process of claim 9, wherein the metal pad comprises a metal stack comprising four different metal levels.

16. The process of claim 15, wherein the metal levels comprise Zirconium, Nickel, Copper and Gold.

17. The process of claim 9, wherein said photoresist layer comprises a thin layer of silicon nitride interposed between an upper layer and a lower layer of photoresist.

18. The process of claim 9, wherein the first insulating layer is polished by chemical mechanical polishing before the at least one first hole is formed.

19. The process of claim 9, wherein the at least one first hole is formed in the first insulating layer by a photoresist etch process.

20. The process of claim 9, wherein at least one portion of the second insulating layer is removed prior to the application of the solder layer.

21. The process of claim 20, wherein the at least one second hole is formed in the photoresist layer above the area in the second insulating layer which has been removed.

22. The process of claim 9, wherein the first insulating layer is at least 2 microns thicker than the at least one metal contact.

23. The process of claim 16, wherein the Zirconium layer is at least 500 Angstroms thick.

24. The process of claim 16, wherein the Nickel layer is at least 750 Angstroms thick.

25. The process of claim 16, wherein the Copper layer is at least 5000 Angstroms thick.

26. The process of claim 16, wherein the Gold layer is at least 750 Angstroms thick.

27. The process of claim 17, wherein the silicon nitride layer is at least 500 Angstroms thick, and the upper and lower layers of photoresist are at least .5 microns thick.

28. The process of claim 9, wherein the solder layer applied is at least 2.33 microns thick.

29. The process of claim 9, wherein the solder area has a diameter less than 100 microns.

30. The process of claim 9, wherein the solder area has a diameter less than 50 microns.

31. The process of claim 9, wherein the solder area has a diameter less than 25 microns.

32. The process of claim 9, wherein the solder area has a diameter less than 10 microns.

33. The process of claim 9, wherein the solder area has a diameter approximately 2 microns.

34. The process of claim 9, wherein the solder area is reflowed to form a solder contact.

35. The process of claim 9, wherein said semiconductor device is an integrated circuit wafer.

36. The process of claim 9, wherein said semiconductor device is an integrated circuit.

37. A method for forming a solder area on a semiconductor device comprising the steps of:

depositing an insulating layer over at least one metal pad formed on the semiconductor device;

depositing a photoresist layer over said insulating layer;

forming at least one hole in the insulating layer and the photoresist layer to expose said at least one metal pad;

applying a solder layer over the photoresist layer and in the at least one hole to from at least one solder area in the hole; and,

removing the photoresist layer and solder layer using a liftoff process while leaving the solder area on the metal pad.

38. The method of claim 37, where the liftoff process is a tape liftoff process.

39. The method of claim 37, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer, and stripping away said tape to remove the solder layer and the photoresist layer while leaving said solder area.

40. A semiconductor device comprising:

a semiconductor structure having at least one metal contact formed on a surface thereof;

a first insulator layer overlying said at least one metal contact;

at least one metal pad overlying said first insulator layer and in contact with said at least one metal contact;

a second insulator layer overlying said at least one metal pad; and,

at least one solder contact formed in the second insulator and in contact with said at least one metal pad, said solder contact having a diameter less than 100 microns.

41. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 50 microns.

42. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 25 microns.

43. The semiconductor device of claim 40, wherein the solder contacts have a diameter less than 10 microns.

44. The semiconductor device of claim 40, wherein the solder contacts have a diameter of approximately 2 microns.

45. The semiconductor device of claim 40, wherein said at least one metal contact is connected to said at least one metal pad by a via hole formed in the first insulator.

46. The semiconductor device of claim 40, wherein the at least one solder contact extends from a top surface of the second insulator to the metal pad by a through hole formed in the second insulator.

47. The semiconductor device of claim 40, wherein the at least one metal pad lies at least partially overtop of the at least one metal contact.

48. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit chip.

49. The semiconductor device of claim 40, wherein the semiconductor device is an integrated circuit wafer.

50. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a module substrate.

51. The semiconductor device of claim 40, wherein the semiconductor device is bonded to a circuit board.

52. A method for forming solder areas on electrical contacts present at a surface of an electrical device, said method comprising the steps of:

depositing a liftoff layer on said surface;

forming respective holes in the liftoff layer to expose said contacts;

applying a solder layer on top of the liftoff layer and in the holes to form solder areas in the holes which are in contact with respective ones of said electrical contacts; and,

removing the solder layer and liftoff layer using a liftoff process while leaving the solder areas.

53. The method of claim 52, wherein the liftoff process comprises applying an adhesive tape overtop of the solder layer, and stripping away said tape to remove the solder layer and the liftoff layer while leaving said solder areas.

54. The method of claim 52, wherein the liftoff layer comprises an insulating layer.

55. The method of claim 54, wherein the insulating layer is a polyimide layer which can be peeled away.

56. The method of claim 52, wherein the liftoff process is a tape liftoff process.

57. The method of claim 52, wherein the electrical device is an integrated circuit chip.

58. The method of claim 52, wherein the electrical device is an integrated circuit wafer.

59. The method of claim 52, wherein the electrical device is a circuit board.

60. The method of claim 52, wherein the electrical device is a module substrate.

61. The method of claim 52, wherein the liftoff layer is photoresist layer.

62. A method of forming contact pads and solder areas on an electrical device comprising the steps of:

depositing a photoresist layer on the surface of an electrical device containing vias;

forming respective holes in the photoresist aligned with said vias;

applying a layer of contact metal to form contacts in the vias and in the holes overlying said vias;

applying a layer of solder to form solder areas on top of the contacts in the holes over said vias;

removing the solder and the contact metal which lies on top of the photoresist layer using a liftoff process, while leaving the solder areas and contacts which lie overtop of the vias.

63. The method of claim 62, wherein the liftoff process is a tape liftoff process.

64. The method of claim 62, wherein the solder areas and contacts are reflowed to form solder ball contacts.

65. The method of claim 62, wherein the electrical device is an integrated circuit.

66. The method of claim 62, wherein the electrical device is a circuit board.

67. The method of claim 62, wherein the electrical device is a module substrate.

ABSTRACT

A method of forming micro solder balls for use in a C4 process is described. The solder balls are formed by laying down a peel-away photoresist layer, forming holes in the photoresist layer to expose electrical contacts, depositing a solder layer over the photoresist, forming solder areas in the holes and then, using a tape liftoff process to remove the solder layer and photoresist layer while leaving solder areas in the holes. The solder areas are then heated to allow solder balls to form.

FIG. 1
PRIOR ART

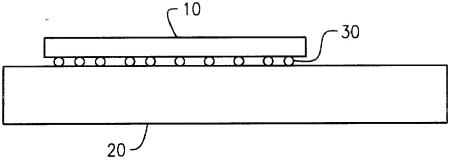


FIG. 2
PRIOR ART

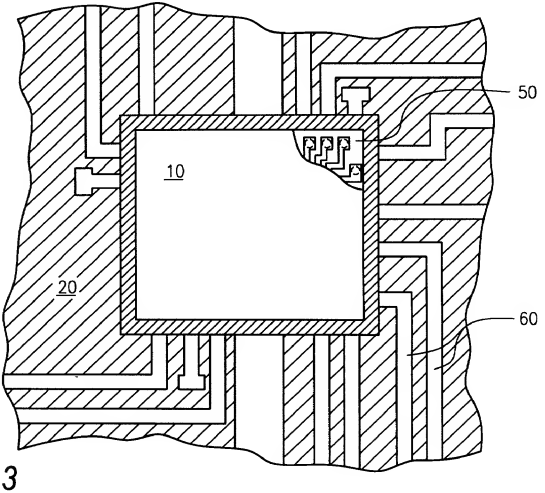


FIG. 3
PRIOR ART

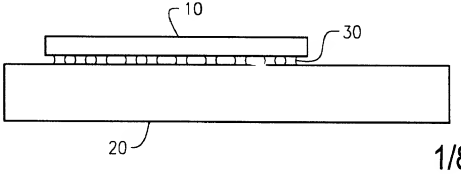


FIG. 4A

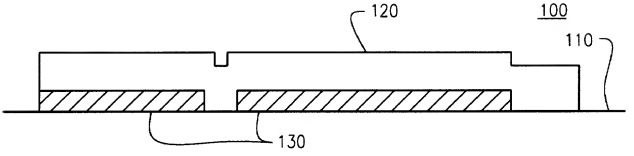


FIG. 4B

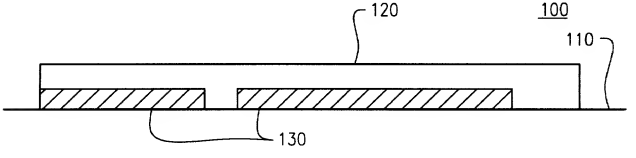


FIG. 4C

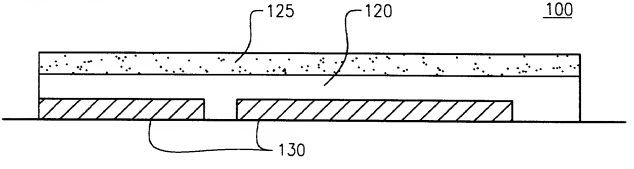


FIG. 4D

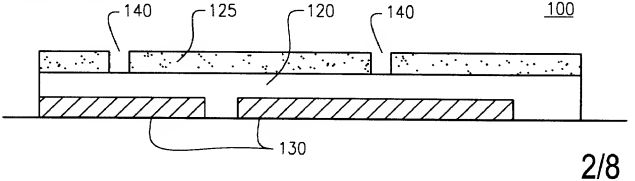


FIG. 4E

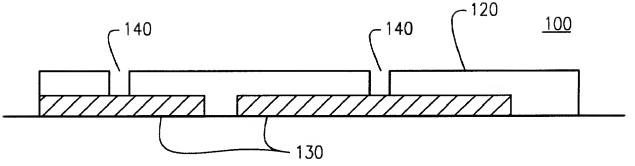


FIG. 4F

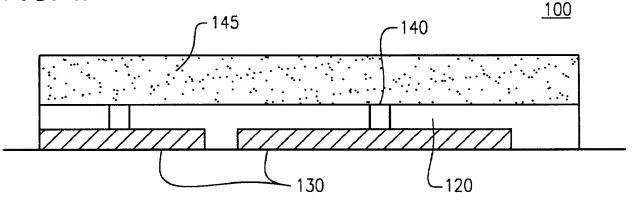


FIG. 4G

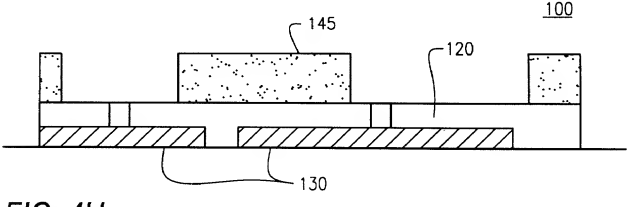


FIG. 4H

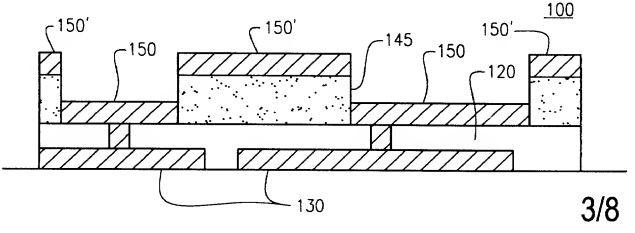


FIG. 4I

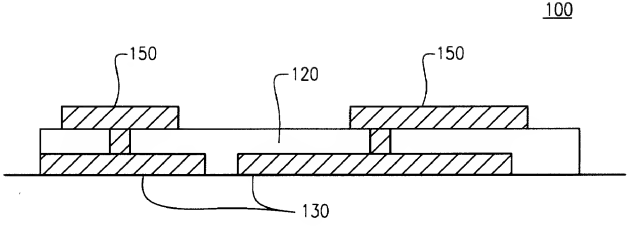


FIG. 4J

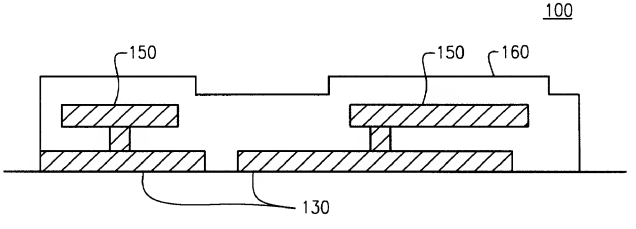


FIG. 4K

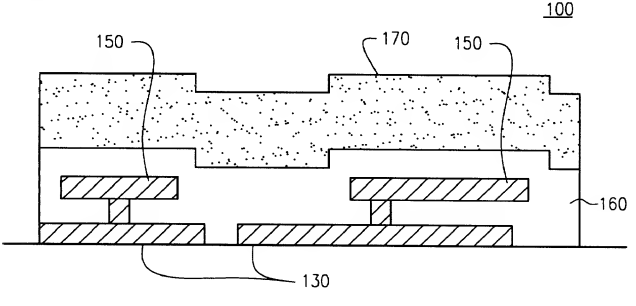


FIG. 4L

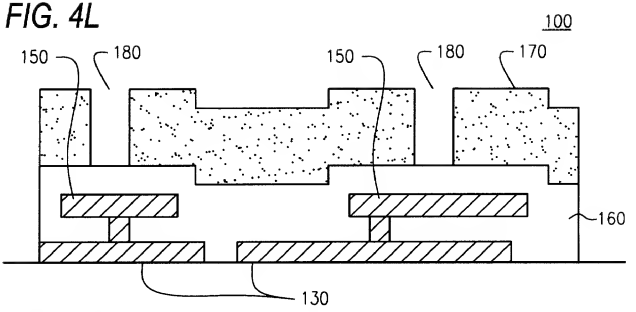


FIG. 4M

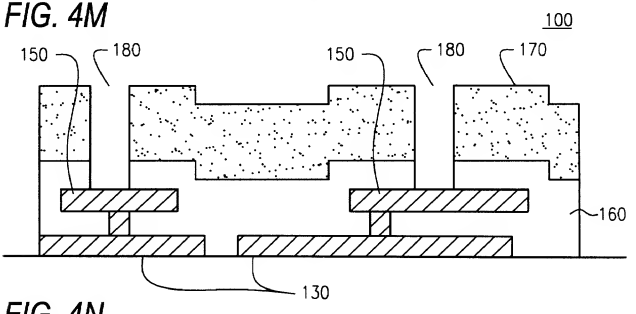


FIG. 4N

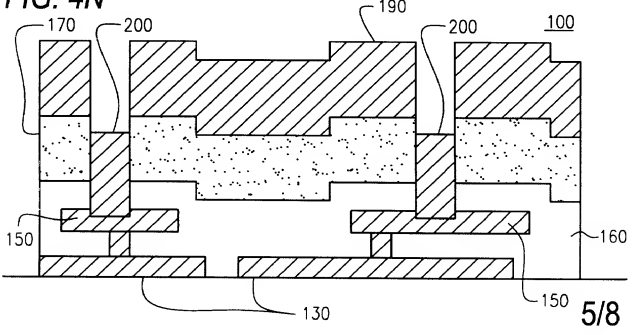


FIG. 4O

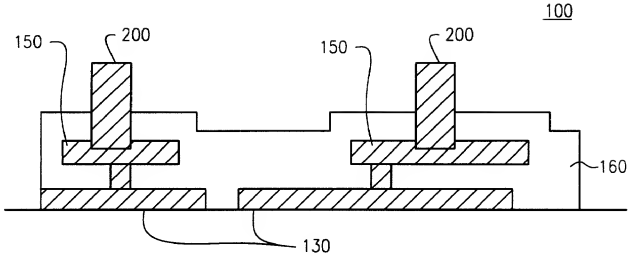


FIG. 4P

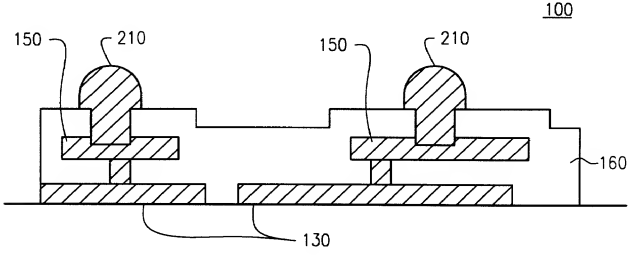


FIG. 4Q

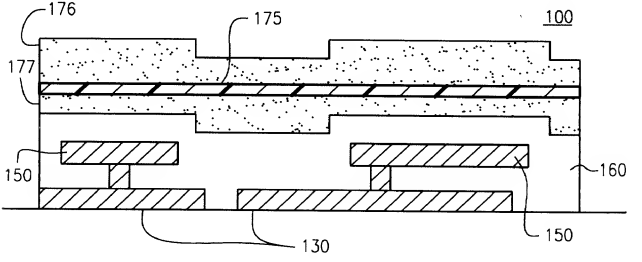


FIG. 5A

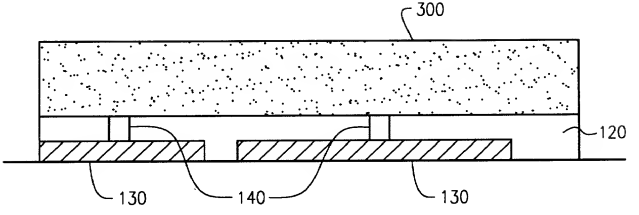


FIG. 5B

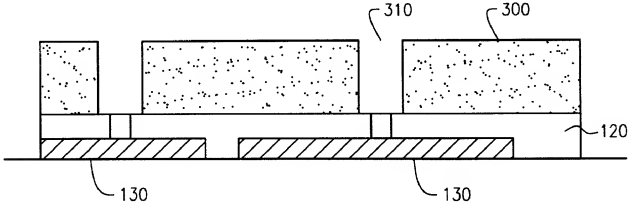


FIG. 5C

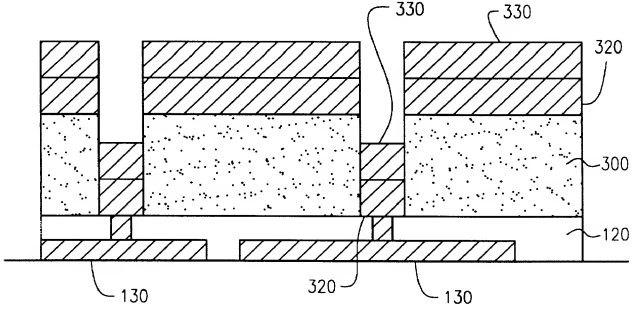


FIG. 5D

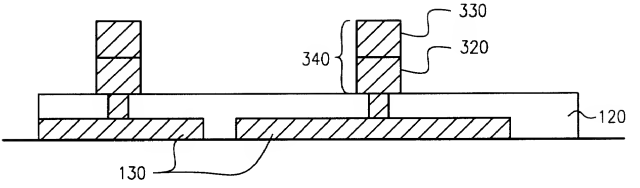
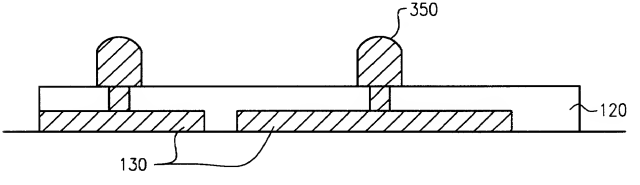


FIG. 5E



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN A C4 BONDING PROCESS.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526. Telephone calls should be made to Thomas J. D'Amico by dialing (202) 828-2232.

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Inventor's signature  Date Aug 11, 1998

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PATENT
Docket No.: M4065.082/P082
Micron No.: 98-0111

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Patent Application
Inventor: Paul A. Farrar

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: METHOD OF FORMING A MICRO SOLDER BALL FOR USE IN A C4 BONDING PROCESS

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; Juliana Haydoutova, P43,313; James M. Heintz, P41,828; Herbert V. Kerner, P42,721; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M. Silbermann, 40,413; Richard Veltman, 36,957 and Darius Gambino, 41,472,

and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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MICRON TECHNOLOGY, INC.

Michael L. Lynch
Chief Patent Counsel
Registration No. 30,871

Dated: May 14, 1998